REMARKS

In response to the Office Action, claims 1- 4 have been amended. New claims 6 and 7 have been submitted for the Examiner's consideration. Accordingly, claims 1-7 are currently pending.

Claim 5 has been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner asserts that claim 5 "appears to be incorrect since the second connecting means (transistors 8 and 9) are not in parallel-connection as recited in claim." Applicant respectfully disagrees and points the Examiner to page 5, lines 4-5 of the specification as originally filed, which recites that "analog switch 6 comprises a pair of FETs of a P channel type and an N channel type, which is connected in parallel."

Claims 1-5 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,466,054 to Kameyama et al. ("Kameyama").

Claim 1 has been amended to recite a complementary signal generator for outputting complementary positive-phase and antiphase signals that vary between a first logical value and a second logical value comprising a positive-phase signal output part and an antiphase signal output part. A signal forming unit outputs a positive-phase intermediate signal that is in phase with an input signal varying between the first logical value and the second logical value to a positive-phase intermediate node, and an antiphase intermediate signal antiphase to the input signal to an antiphase intermediate node. A first connecting means, connected among the positive-phase intermediate node, the antiphase intermediate note, the positive-phase signal output part, and the antiphase signal output part and having a first control terminal for receiving a first control signal produced in synchronism with a state change of the input signal from the first logical value to the second logical value, simultaneously transfers the second logical value of the positive-phase intermediate signal and the first logical value of the antiphase intermediate signal to the positive-phase signal output part and the antiphase signal output part respectively.

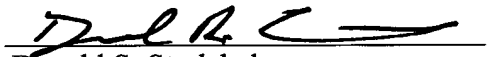
Amended claim 1 clearly recites that a first connecting means has "a first control terminal for receiving a first control signal." The present invention simultaneously transfers the signals applied to the positive-phase intermediate node and the antiphase intermediate node. Thus, the

complimentary signal can be produced at the positive phase signal output part and the antiphase signal output part.

Kameyama does not disclose "a first connecting means .....having a first control terminal for receiving a first control signal produced in synchronism with a state change of the input signal from the first logical value to the second logical value," as recited in claim 1. Kameyama merely discloses MOS FETs 103 and 102 having fixed voltage potentials VD1 and VS1 applied to gate terminals thereof. Thus, Kameyama does not disclose the above recited claim language. Therefore, because each and every limitation recited in claims 1-7 is not found within the four corners of Kameyama, the claims are allowable.

A prompt passage to issuance is therefore earnestly solicited.

Respectfully submitted,



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